CLEAN COPIES OF THE CLAIMS:

12. (Amended) A semiconductor device including a memory cell region and a peripheral circuit region, comprising:

a semiconductor substrate having a major surface;

an insulating film, having an upper surface, being formed on said major surface of said semiconductor substrate to extend from said memory cell region to said peripheral circuit region;

a capacitor lower electrode assembly, including first and second lower electrodes being adjacent to each other through a part of said insulating film, being formed on said major surface of said semiconductor substrate to extend up to a vertical position substantially identical to that of said upper surface of said insulating film in said memory cell region; and

a capacitor upper electrode being formed on said capacitor lower electrode assembly through a dielectric film to extend onto said upper surface of said insulating film, said upper electrode being formed on an interior region of each of the first and second electrodes,

said capacitor lower electrode assembly including a capacitor lower electrode part upwardly extending in opposition to said capacitor upper electrode and having a top surface and a bottom surface.

15. (Amended) The semiconductor device in accordance with claim 12, comprising ~~said~~ dielectric film being formed between one of:

at least a side surface of said capacitor lower electrode part and said insulating film, and

at least only a part of said bottom surface of said capacitor lower electrode part and said insulating film.